

DSP for ATE Case Study

Background

A major ATE vendor set out to build a new mixed-signal tester based on their very successful VLSI tester. This tester categorized as a Big-D/Little-A tester had some very complex requirements stemming from the legacy digital tester. This project called for people with an in-depth understanding of building systems as well as a good understanding of the ATE testing methodologies, runtime software, digital signal processing and client-server technologies.

The Project

The engineers involved in this project did a comprehensive requirements study and wrote the functional and detailed design specifications for the runtime system and the DSP sub-system. The DSP sub-system was made up of multiple cards each of which housed two commercially available DSP processors and associated capture memory for both digital and analog data. The DSP card was also capable of sourcing waveforms. An additional requirement for this project called for a DSP simulator that would run on the host processor, in the absence of the actual tester. The latter served as a good mechanism to allow engineers to debug their ATE test programs in the absence of the actual tester, a very precious commodity due to the high cost.

The software consisted of the host software that communicated with any of the target DSP cards, the executive that ran on the DSP processors and the simulator that ran on the host processor. Speed of testing was very critical to the success of this project.

Highlights

- Small memory footprint executive to conserve memory
- High throughput testing of devices with very small overhead from executive
- Functional simulator of DSP hardware on host processor
- Low latency in communication overhead between host and target
- Optimal buffer management
- Servo-loop testing of devices using software